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(54) **METHODS FOR FORMING INTEGRATED CIRCUITS WITHIN SUBSTRATES**

(75) Inventors: **Mark E. Tuttle**, Boise; **Rickie C. Lake**, Eagle, both of ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(58) **Field of Search** 438/19, 42, 64, 438/125, 126; 29/840, 846, 852, 837, 848, 849, 850; 264/272.17

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Primary Examiner—Caridad Everhart
(74) *Attorney, Agent, or Firm*—Wells, St. John, Roberts, Gregory & Matkin, P.S.

(57) **ABSTRACT**

The invention includes methods for forming integrated circuits within substrates, and embedded circuits. In one aspect, the invention includes a method of forming an integrated circuit within a substrate comprising: a) providing a recess in a substrate; b) printing an antenna within the recess; and c) providing an integrated circuit chip and a battery in electrical connection with the antenna. In another aspect, the invention includes a method of forming an integrated circuit within a substrate comprising: a) providing a substrate having a first recess and a second recess formed therein; b) printing a conductive film between the first and second recesses and within the first and second recesses, the conductive film forming electrical interconnects between and within the first and second recesses; c) providing a first electrical component within the first recess and in electrical connection with the electrical interconnects therein; d) providing a second electrical component within the second recess and in electrical connection with the electrical interconnects therein; and e) covering the first electrical component, the second electrical component and the conductive film with at least one protective cover. In another aspect, the invention includes an embedded circuit comprising: a) a substrate having a recess therein, the recess having a bottom surface and a sidewall surface joined to the bottom surface; b) interconnect circuitry formed on the bottom and sidewall surfaces; and c) an integrated circuit chip within the recess and operatively connected to the interconnect circuitry.

18 Claims, 7 Drawing Sheets